

In re KNOWLTON, 178 USPQ 486 (CCPA 1973)

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**(CCPA)
178 USPQ 486**

Decided July 26, 1973

No. 8896

U.S. Court of Customs and Patent Appeals

Headnotes

PATENTS

1. Claims — "Means" claims (§ 20.65)

Specification — Sufficiency of disclosure (§ 62.7)

Sentence of 35 U.S.C. 112 authorizing recitation of claim element in terms of "means" does not add any additional description requirement to that set forth in first paragraph of section; however, while sentence is permissive, it cannot be read as creating an exception either to description requirement of first paragraph or to definiteness requirement in second paragraph; means-plus-function language can be used in claims, but claims must still accurately define the invention; invention claimed must be described somewhere in specification.

2. Specification — Sufficiency of disclosure (§ 62.7)

It must be borne in mind that disclosure need not only be full, clear, and exact to satisfy 35 U.S.C. 112, but it also must be concise; disclosure is directed to those skilled in the art; amount of precision necessary in any given case is always a matter of degree; absent special circumstances, it is not required that every nut, bolt, and rivet used in mechanical inventions be described, or, in chemical cases, that electron orbital patterns for claimed compound be set forth.

3. Claims — Including same element twice (§ 20.50)

Claims — "Means" claims (§ 20.65)

Apparatus claim reciting both functions of involved element or circuit in means-plus-function language is adequately supported if apparatus is adequately described; it may be that claim is rendered indefinite by multiple inclusion of same element or circuit, but that does not necessarily follow.

Particular patents—List Processor

Knowlton, List Processor, claims 3, 7, and 10 to 14 of application allowed; claims 1, 2, 5, 6, 8, 9, and 15 to 22 refused.

Case History and Disposition:

Appeal from Board of Appeals of the Patent Office.

Application for patent of Kenneth C. Knowlton, Serial No. 598,503, filed Dec. 1, 1966; Patent Office Group 237. From decision rejecting claims 1 to 3 and 5 to 22, applicant appeals. Affirmed as to claims 1, 2, 5, 6, 8, 9, and 15 to 22; reversed as to claims 3, 7, and 10 to 14.

Attorneys:

ROBERT O. NIMTZ, Madison, N. J., for appellant.

S. WM. COCHRAN (JERE W. SEARS of counsel) for Commissioner of Patents.

Judge:

Before MARKEY, Chief Judge, and RICH, ALMOND, BALDWIN, and LANE, Associate Judges.

Opinion Text

Opinion By:

BALDWIN, Judge.

This appeal is from the decision of the Patent Office Board of Appeals affirming the examiner's rejection of claims 1-22. all the claims in appellant's application. ¹

The Invention

Appellant's invention relates to a system for computer processing of list information, i.e., items of information which are related or have

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characteristics in common, such as business inventories, personnel files, business accounts, etc. The application states:

For many applications, data items can be easily linked by their mere contiguity, such as a list on a single sheet of paper. In other cases, however, items are added and deleted at various times, and the interrelationship between items is not a simple linear one. In an inventory list, for example, a hierarchy must be maintained with each item linked in one way to the items out of which it is made, and linked in another way to that item of which it forms a part. In addition, cross referencing, for example, to other items which are similar in structure or origin may also be required. While separate lists could be maintained to express all of these relationships by duplicating appropriate items on the different lists, such an organization is wasteful of space and unmanageable with even moderately-sized item sets.

A more useful listing includes each item only once, but includes with the data item "links" to all other relevant items. Since these "linkages" have many different significances, the links likewise have distinguishable characteristics.

In the present invention, a data item is entered into a unitary block of storage space along with all of the necessary links. Since the number of linkages is variable as well as the number and size of data items, the size of the storage blocks is likewise made variable. In order to distinguish the various linkages, they are entered into different fields in the storage blocks. A field, in this connection, is defined as any contiguous set of single bit storage positions within the block. Since the blocks are naturally divided into "words" (i.e., standard length contiguous bit positions), fields are also defined to include only portions (or the whole) of single words. The various links then constitute address pointers to the linked blocks.

In order to utilize the available storage capacity most efficiently, so-called "free storage" lists are likewise maintained. These are singly-linked lists of the storage blocks available in the system, but not yet called into use. Since different size blocks are available, a separate list is provided for each size of block. The entire available storage area may, for example, initially be assembled into a single free storage list of blocks of the maximum size. A block of this size can then be obtained merely by removing it from the free storage list. If a smaller sized block is required, larger blocks are split in two until a block of the appropriate size is available. Finally, when blocks are no longer needed, they can be returned to the appropriate free storage list for future use.

The application sets out schematic block diagrams related to various aspects of the invention. Figure 1 is typical, and shows how the memory blocks of various sizes are obtained:

The application also contains descriptions of the drawings, in which the relationships between the depicted components of the invention are generally described. However, what appellant contends is a complete disclosure of the preferred embodiment of the invention is made up of a number of computer program listings for use of the invention with a general purpose digital computer, and descriptions of how the listed programs work. The specification refers to the IBM 7094 Data Processing System as one type of apparatus which could process the listed computer programs.

The first listing which appears in the application is entitled "Storage Allocator," and the first part of that listing appears as follows on page 488.

Following each program listing, there is an explanation of how the listed program works. While some of these explanations are more detailed than others, we find that the explanation of the above-quoted portion of the first listing is sufficiently representative for an understanding of the case:

The 1-block procurer * * * is implemented by the "GET.1" subroutine, entered by a transfer to the location labeled GET.1. The first instruction (SXA *+ 8, 4) is a direction to save the contents of the indicated index register, in this case, index register 4, in the location "*+8," which is interpreted as the location eight instructions after the current instruction. This is instruction 9 in the GET.1 subroutine, and the index register contents are stored in the address field of instruction 9 reserved by the double asterisk. Since index register four will be used in the GET.1 subroutine to hold a reference address when transferring to another subroutine, the original contents must be saved. These contents represent an address in the main program from which the transfer to the GET.1 subroutine took place and to which control is to be returned after execution of the subroutine.

Instruction 2 in the GET.1 subroutine (NZT 1.S) is a direction to test the contents of location 1.S for a zero. If a zero is found there, the next instruction is executed. If anything but zero is found, the next instruction is skipped. The location 1.S is the head of the 1-block free storage list. If there are any 1-blocks on this list, location 1.S

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holds a pointer to the first block. If there are none, location 1.S holds zero. The test at

instruction 2 ascertains which is the case, and, if a zero is found (no 1-block available), instruction 3 (TSX SPLIT2, 4) is executed. This instruction is a transfer to the subroutine "SPLIT2" corresponding to the 2-block splitter 16 in FIG. 1. Before transferring, the current location (of instruction 3) is stored in index register 4 to provide a return address from the SPLIT2 subroutine. The SPLIT2 subroutine returns with the addresses of two 1-blocks, the address of the first in location 1.S, and the address of the second in the first.

Instruction 4 (LDQ 1.S) loads the 1-block address in location 1.S into the Multiplier-Quotient Register. Instruction 5 (CAL* 1.S) places the address in the 1-block whose address is in location 1.S into the Accumulator Register. This indirect addressing facility (indicated by the asterisk after CAL) is available in many general purpose computers. If not available, the same effect can be obtained by explicitly getting the address and using it for access.

Instruction 6 (STZ* 1.S) puts all zeros in the location whose address is in location 1.S. This, of course, is the first 1-block. This block is cleared so as to be ready for use when delivered back to the main program.

Instruction 7 (STA 1.S) stores the address which is in the Accumulator Register into location 1.S. As noted in instruction 5, this address is the address of the second 1-block in the list. In effect, the first 1-block has been removed from the free storage list by replacing the address of the first 1-block with the address of the second 1-block in location 1.S (the head of the free storage list).

Instruction 8 (XCL) exchanges the contents of the Accumulator Register and the Multiplier-Quotient Register. This leaves the address of the first 1-block, loaded into the Multiplier-Quotient Register in instruction 4, in the Accumulator Register. This is where it is expected to be found when returning from the GET.1 subroutine.

Instruction 9 (AXT **,4) was discussed above. This instruction loads the return address back into index register 4 to permit a return to the main program.

Instruction 10 (TRA 1,4)) transfers control back to the calling program. It transfers control to the first location after the location stored in index register 4.

Appellant states that "the claims are all couched in the 'means-plus-function' claim format sanctioned by the third paragraph of 35 U.S.C. § 112." He further states that most of them "call for means for organizing a memory into storage blocks, means for specifying fields in such storage blocks, base registers for holding pointer signals to the blocks, and processing means using the pointer signals for operating on the contents of specified fields." Claim 1 is exemplary (paragraphing ours):

1. A linked list processor comprising a memory,
means for establishing blocks of storage within said memory,

means for specifying fields within said blocks for storing data signals and linking signals.

said fields being of arbitrary size and location within said blocks.

a plurality of base registers for storing linking signals to prescribed ones of said blocks, and

means for accessing and processing the contents of any prescribed field in said memory.

The Rejections

The board sustained rejections of all the claims by the examiner as based on an inadequate disclosure and as failing to particularly point out and distinctly claim what appellant regarded as his invention, relying on paragraphs 1 and 2, respectively, of 35 U.S.C. 112. It also sustained the rejection of claims 1-5, 12, 14, 15, 17 and 19-22 as fully met by any of patents to Tomasulo et al. (Tomasulo), ² Anderson et al. (Anderson) ³ or Shimabukuro ⁴ under 35 U.S.C. 102 and of the remaining claims as obvious under 35 U.S.C. 103 over those references further in view of patents to Bauer ⁵ and Mullery. ⁶ The board reversed certain other prior art rejections, as well as a rejection of the claims as being directed to "nonstatutory subject matter."

The Section 112 Rejections

The examiner rejected all of the claims "on the basis of insufficient and inadequate disclosure." The examiner considered that appellant's application did not disclose structure upon which the claims could be based. The examiner stated:

Each and every instruction in appellant's program does not "uniquely and unambiguously identify an apparatus configuration" * * *. As an example, the sequence of 10 instructions designated as "Block Procurer"

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* * * shows that each and every instruction listed therein is for the purpose of manipulating data and not for the purpose of identifying any apparatus configuration * * *

The examiner also noted that "there is a substantial repetition or overlap of the same program instructions" being used in all of appellant's program listings. Intermixed with the above rejections were the examiner's contentions that appellant had failed to set forth the "best mode" of his invention.

The board started out by accepting appellant's disclosure as being *adequate* "insofar as the programs detailed in the specification would be effective ultimately to condition that computer to carry out appellant's procedure of allocating memory locations within the computer * * *." After noting that the specification did not sufficiently disclose any specially constructed hardware for

carrying out the invention, the board stated:

Claim 1, as reproduced above, clearly carries out appellant's expressed intent to preempt for himself every possible hardware configuration that would give the same ultimate result as the one asserted for his programming of a general purpose computer, notwithstanding the absence of an adequate teaching of any such hardware disclosure by his specification.

In our view the third paragraph of 35 U.S.C. 112 sets the bounds for construing claims couched in terms of a means for performing a stated function. Coverage can extend only to the apparatus disclosed, which here would be a programmed general purpose computer, and to equivalents thereof, which would not be all possible apparatus for attaining the same result without regard to whether or not the disclosed apparatus, not the ultimate result, would suggest the equivalent apparatus. Since a programmed general purpose computer bears no discernable apparatus relationship to a specially constructed machine, the broad sweep of the appealed claims finds no supporting disclosure by appellant. By specifically directing his claims to be construed as for apparatus not adequately disclosed, appellant is overclaiming his invention so as to deter, rather than promote, progress in the art.

Additionally, each of the appealed claims calls for a series of means for performing specified operations on data to be stored or recalled in a linked sequence in which each means is stated to be in combination with each of the other means set out by the claims. As the examiner has pointed out, the same instructions, and presumably the same apparatus in the programmed computer, would be required to perform each of the several functions. When this same apparatus is reconnected through each instruction of the program to carry out different functions, the means for performing the prior function no longer is in existence so that there never exists at the same time a means for performing both successive functions as the appealed claims allege by claiming a combination thereof in the same way that a special purpose computer could be claimed. Following the analogy that a programmable computer is a warehouse of parts that are connected and reconnected only by the execution of successive program instructions, there is no more a combination of the two apparatus configurations than there would be a combination, in the usual sense, between a radio transmitter and a radio receiver when the latter has been constructed from various parts taken from the former. The successive apparatus configurations are related to each other only by a procedure of reconnection and not by any structural relationship there between.

The examiner based his rejection of the claims under the second paragraph of section 112 on the following reasoning:

Applicant specifically states that his invention is a program or series thereof, but such applicant is confusing the issue by couching his claims in means plus function language. Such disclosed programming must be changed to method steps to be properly

claimed.

The board also sustained this rejection, and its reasoning was similar to the examiner's:

This leads to the examiner's second rejection under 35 U.S.C. 112 as for failure to point out that which appellant considers to be his invention. Although appellant does state that he regards both a programmed general purpose computer and a specially constructed apparatus to constitute his invention, we note the following on page 10, lines 2-5 of the specification:

"* * * Insofar as the present invention is concerned, the essence of applicant's contribution lies in the cooperative effect of the functional means, and not in any specific implementation of these functions."

Since each of the various functions involved in appellant's invention is required to be performed serially and appellant asserts no reliance on particular apparatus to perform these functions, he has, in effect, acknowledged that his invention is in the procedure or method and not in the apparatus that is the subject of his claims.

The Prior Art Rejections

In effect, appellant concedes that the section 103 rejection is sustainable *if* "appellant's

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basic combinations" are found to be obvious in view of the primary references. Further, as the board noted, Tomasulo is by far the most pertinent reference, both with regard to the section 102 rejection and the section 103 rejection. We therefore see no reason to burden the opinion with detailed treatment of the other references.

Like appellant's application, Tomasulo was concerned with the efficient allocation of memory space in computer memories. Among the recited objects of the Tomasulo invention are "to pool empty memory locations for use by input devices as needed without searching," and, "to provide means for assigning, to a plurality of inputs empty memory locations from a queue of all available empty memory locations and for assigning to said queue empty memory locations freed by any of a plurality of outputs." The invention is generally described by Tomasulo, with inserted references to Figure 1a as follows:

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These objects are achieved, in one embodiment of the invention, by apparatus including a plurality of input/output lines [01, 02, etc.], character assembly means [3] for each line, a memory [2] having a plurality of empty message assembly sections allocatable to said lines as needed, and means [1] for holding an inventory word for designating the beginning and the end of a queue of available empty locations in said

memory. For purposes of explanation it is convenient to picture information entering and leaving on the input/output lines as serial signals (bits), groups of which form characters of information. A message comprises a plurality of characters. The serially received bits are assembled into character groups in a character assembler [3] and are then forwarded to successive locations in empty message assembly sections (or areas or blocks) of the memory. Each memory section comprises a plurality of locations, each location being capable of storing a number (one, in this simplified example) character. The last character location in each memory section is used to store a designation indicating the location of the beginning location of some other memory section [BLOCK CONTROL CHARACTERS]. Initially all empty memory sections to be used for message assembly are chained together (or pooled) into a queue in any convenient sequence, the last location of each section specifying the next empty memory location.

Each input/output line is assigned a message assembly area for assembling incoming messages, or as a source for outgoing messages. During output, when a message portion stored in a memory section is sent out on a line, a designation of the newly emptied section is added to the end of the queue. Therefore, a current inventory of all available empty sections is maintained for the common use of all lines during both input and output. A designation of the current

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first memory section in the queue is indicated in one portion of an inventory word [NEXT BLOCK], and a designation of the current last memory section in the queue is placed in another portion of the inventory word [END BLOCK]. Each time that an empty section is needed by an input line for message assembly, the first memory section in the queue indicated by the inventory word is assigned to the line. The chaining character at the end of the newly assigned section replaces the first memory section designation in the inventory word, since it indicates the next empty available section in the queue. A designation of the first location in the newly assigned section is placed in the last location of the previous section allotted to the input line, so as to indicate where the input message is continued. Whenever a newly emptied memory section (its contents having been sent on an output line) becomes available, a designation of its location is placed in the inventory word last memory section portion, and also in the last character location of the memory section indicated by the inventory word portion being replaced. In this way the queue is extended and its new end is indicated.

In summary, the inventory word keeps track of the beginning and end of a chain of empty memory sections available for message assembly as needed. Empty sections are removed from the beginning of the chain as needed, and are added to the end of the chain as available. The inventory word is adjusted to always indicate the limits of the chain. The words "queue," "pool" and "chain" describe the empty memory sections (or "areas" or "blocks") available for allocation (or "assignment" or "allotment") to input lines.

Opinion

35 U.S.C. 112 reads in its entirety as follows:

112. Specification

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention. A claim may be written in independent or dependent form, and if in dependent form, it shall be construed to include all the limitations of the claim incorporated by reference into the dependent claim.

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

The first paragraph thus requires, first, that the specification describe: (1) the invention; (2) the manner of making the invention; and (3) the manner of using the invention. How must these things be described? They must be described "in such full, clear, concise, and exact terms as to enable any person skilled in the art" to understand them. In connection with item (1), the specification must indicate to the skilled artisan what the invention is. In connection with items (2) and (3), the skilled artisan must sufficiently understand the manner of making and the manner of using the invention as to be *enabled* to make and use the invention. What invention do these requirements deal with? The invention subject to scrutiny by the Patent Office, or by the courts, is the invention *defined by the claims* called for by the second paragraph of section 112. The first paragraph also requires that the "best mode contemplated by the inventor of carrying out his invention" be set forth in the specification.

The second and third paragraphs of section 112 deal with the claims. The first sentence of the second paragraph contains three requirements. The first is, of course, that the specification conclude with claims. The second is that the claims must particularly point out or identify that subject matter which appellant regards as his invention. The last requirement is that the claims must distinctly define that subject matter, that is, their terminology must be clear and accurate so as to define the metes and bounds of their coverage.

The remaining two sentences deal with *permissible* forms of claiming. It is unnecessary to deal with the first of these here.

[1] The last sentence contains no language which states or implies a further burden on the *applicant*. It allows the applicant to use claim language which recites a claim element in terms of "means or step for performing a specified function." If the applicant chooses to use such language, the statute instructs the interpreter of the claims, e.g., the Patent Office or the courts, as to how such language shall be interpreted. It states that such language "shall be construed to cover the corresponding structure, material, or acts *described in the specification* and equivalents thereof." The emphasized

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language does not add any *additional* description requirement to that set forth in the first paragraph of the section. On the other hand, while the sentence is clearly permissive, it cannot be read as creating an exception either to the description requirement of the first paragraph, discussed *supra*, or to the definiteness requirement found in the second paragraph of section 112. Means-plus-function language can be used in the claims, but the claims must still accurately define the invention.⁷ Such is the plain meaning of the statutory language. What meager legislative history of section 112 exists, supports our interpretation.⁸

Thus, if the board's language in this case means that the third paragraph of section 112 contains a separate and additional description requirement, as the solicitor appears to argue, we must disagree. However, we *agree* with the board that *the invention claimed* must be described somewhere in the specification. At most, our difference with the board amounts to a disagreement as to the source of that requirement. Thus the first question before us narrows down to whether the apparatus which is the subject of appellant's claims is described in appellant's specification in the manner required by the first paragraph of § 112.

It appears to us that the crux of the examiner's position was that the specification was essentially devoid of disclosure of *apparatus* which would comply with the claims. At times the examiner seemed to imply that in order to satisfy the statute appellant's disclosure would not only have to include a detailed description of the circuits contained in the proprietary computer referred to by appellant, but would also have to include a detailed description of the physical state such circuits would be placed in by the disclosed program. The board's position was a variation on the same theme, a major premise being that "a programmed general purpose computer bears no *discernable apparatus relationship* to a specially constructed machine * * * [emphasis added]." A second rationale underlying the "insufficient support" rejection was first indicated in the examiner's answer and was more fully developed by the board. It is to the effect that no apparatus fitting the claims was described because if one applied the claims to appellant's disclosure, the identical pieces of hardware contained in the proprietary computer would necessarily fulfill more than one of the functions contained in the means-plus-function recitations of the claims. In other words, the contention is that the description is improper because the claims cannot be read on it without interpreting the claims as including multiple recitations of the same elements. To buttress this argument, it was pointed out that during operation of appellant's program not all of the recited "means" are likely to be in existence simultaneously.

We take both of these rationales to be under the heading of allegations that appellant's disclosure fails to set forth the invention in such full, clear, concise and exact terms as to allow the skilled artisan to understand what the invention is. We have carefully reviewed the disclosure in the present case, and we conclude that the rejection is not sustainable in this case on either rationale.

[2]In the first place, any allegation that the specification fails to disclose *any* apparatus at all, but only a programming *method*, is totally untenable. Not only does the specification refer to the IBM 7094 Data Processing System, but it also generally discloses such hardware as the memory and base registers which are recited in the claims, and such more specific hardware items as index registers, addressed memory locations, "Multiplier-Quotient Registers," "Accumulator Registers" and others. It is readily apparent, from indications in the present specification and from the level of the art established by the references of record, that those skilled in the art to which the present application is directed would know what types of hardware are designated by these terms and further that the necessary hardware was available. Most important, the disclosure in this case does not merely consist in a sketchy explanation of flow diagrams or a bare group of program listings together with a reference to a proprietary computer on which they might be run. Rather, the disclosure before us goes into considerable detail in explaining the interrelationships between the disclosed hardware elements, as exemplified by the description of the functioning of the "1-Block Procurer" quoted above. True, appellant did not give a description in minute detail of the circuitry which results when his program is loaded into the computer. For example, he did not precisely identify exactly which memory elements are used in his particular 7094 computer to store the first instruction in his "GET.1" subroutine, nor did he describe the direction of magnetization those memory elements take in order to store that first instruction, nor did he describe the precise conductive element or elements which connect those memory elements to his index register 4. However, it must be borne in mind that the disclosure need not

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only be full, clear and exact to satisfy the statute, it must also be concise, and that the disclosure is directed to those skilled in the art. The amount of precision necessary in any given case is always a matter of degree. Absent special circumstances it is not required that every nut, bolt and rivet actually used in mechanical inventions be described, or, in chemical cases, that the electron orbital patterns for a claimed compound be set forth. Appellant contends that his specification is sufficient to place the skilled artisan in possession of the claimed inventions. The level of skill in the art which is indicated by the record before us supports that contention.

As to the second rationale, it appears to us to be based on the premise that each means-plus-function element in a claim can *only* be read on a single, complete mechanical element of the invention, which performs the recited function without aid from other elements of the invention. Thus the board and the examiner considered that the means-plus-function recitations in the claims were not supported by the disclosure because some of the hardware disclosed, for example index register 4, will perform or assist in performing *several* of the

functions listed in those means-plus-function recitations.

[3]We find that the application describes and identifies apparatus combinations which perform each of the functions called for by the means-plus-function recitations of the claims, and further describes how those combinations are made, and that therefore the claims are adequately supported by the specification. The role played by appellant's index register 4, for example, in establishing blocks of storage within a memory is described in the specification and it, together with the other elements necessary to perform that function, also described, does support the claim recitation "means for establishing blocks of memory within said memory." As appellant points out, the board's complaint that "there never exists at the same time a means for performing both successive functions" is inconsistent with the fact that when appellant's program is fully loaded into the computer the stored pattern of signals transforms the unprogramed machine into a new structure, with all the necessary hardware elements being physically interrelated so as to enable them to perform their specified functions. See *In re Bernhart*, 57 CCPA 737, 742, 744, 417 F.2d 1395, 1399, 1400, 163 USPQ 611, 615, (1969). Indeed, the rejection before us is very similar to the section 112 rejection which the board overturned in *Bernhart*. See 57 CCPA at 741, 417 F.2d at 1398, 163 USPQ at 614. The situation before us is not analogous to a radio receiver which "has been constructed from various parts taken from" a radio transmitter, as the board indicated. It is more analogous to a *combination* transmitter-receiver in which a single element, or a part of the circuitry, plays a different role depending on whether the instrument is being used to transmit or receive. An apparatus claim reciting both of the functions of the involved element or circuit in means-plus-function language is adequately supported if the apparatus is adequately described. It may be that the claim is rendered indefinite by the multiple inclusion of the same element or circuit, but even that does not *necessarily* follow. *Techler v. Norstrud*, 475 F.2d 1192, 177 USPQ 390 (CCPA 1973); *In re Kelley*, 49 CCPA 1359, 305 F.2d 909, 134 USPQ 397 (1962); *Palmer v. United States*, 423 F.2d 316, 163 USPQ 250 (Ct. Cl. 1969). At any rate, we again note that no rejection of these claims for indefiniteness is before us.

The board did not mention the examiner's complaints regarding the best mode requirement, but it affirmed the rejections "[f]or the reasons set forth above as well as for the reasons set forth by the examiner in his answer and in the initial and final rejections incorporated therein by reference and not overruled by us * * *." We are not even sure that the examiner's complaints with regard to the best mode were intended to amount to a separate rejection. However, treating them as a rejection for the sake of completeness, we note that they were based on alleged inadequacy of the description of the mode disclosed, for the same reasons as dealt with above, and were not based on any allegation that the mode disclosed was not the best one contemplated by appellant. Thus, for the reasons discussed above, this rejection too must fall.

With regard to the rejection based on the second paragraph of section 112, we disagree that the language from appellant's specification which was quoted by the board amounts to an acknowledgment "that his invention is in the procedure or method and not in the apparatus that is the subject of his claims." At any rate, even if that language amounted to such an acknowledgment or admission, at best that admission constitutes some evidence that the claims were directed to something other than what appellant regards as his invention, and such evidence

would be completely refuted by the rest of the application including the claims as filed, as well as by appellant's position throughout the prosecution of this case, all of which indicate that the invention was considered to be *apparatus* for processing list information.

The Prior Art Rejections

In his brief before the board, appellant characterized the Tomasulo reference as follows:

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The Tomasulo patent is directed to a storage allocator which is quite similar to appellant's FIG. 1 in many respects. Just as in appellant's arrangements, Tomasulo "chains" unused memory blocks together by means of pointers to form a linked list of available memory blocks. Also just as in appellant's arrangement, Tomasulo obtains an available message block whenever it is required and returns it to the available list when it is no longer required. Tomasulo does not show, however, [1] any arrangement for providing storage blocks of different sizes nor [2] for splitting or recombining blocks, as taught by appellant. Tomasulo is thus directed to one sub-combination of appellant's overall invention and moreover, does not even anticipate all of the elements of that sub-combination.

In response to the first alleged Tomasulo deficiency, the board pointed out that "[s]ince the claims do not specify that the fields or blocks be of any specified size, it is solely a matter of semantics that a 'block' of memory in the reference be considered as a double word and a field as a single word in the 'block'." The solicitor exemplified this reasoning in applying claim 1 to the Tomasulo reference, pointing out, for example, that the instantly recited "block" corresponds to a linked plurality of the memory locations which Tomasulo arbitrarily designates as "blocks." The solicitor's reading also correlates Tomasulo's "block control characters" with the instantly recited "plurality of base registers."

We agree with the Patent Office on this point. We find nothing in the extremely broad language used which prevents such a reading of the claims.

With regard to appellant's second point concerning Tomasulo, the board stated that Tomasulo shows a memory "which may be subdivided at will by the usual addressing instructions into fields or blocks of any arbitrary size * * *." While that may be so, there is nothing in Tomasulo or the other references which discloses or suggests both means for dividing the storage block and for recombining said blocks, as is required by claims 3, 7, and 10-14. Thus, while we affirm the prior art rejections of claims 1, 2, 5, 6, 8, 9, and 15-22, we must reverse the rejections of claims 3, 7, and 10-14.

In summary, the rejection of claims 1, 2, 5, 6, 8, 9, and 15-22 is *affirmed*. The rejection of claims 3, 7, and 10-14 is *reversed*.

Footnotes

Footnote 1. Serial No. 598,503, filed December 1, 1966.

Footnote 2. U. S. Patent No. 3,241,125, issued March 15, 1966, on an application filed May 22, 1962.

Footnote 3. U. S. Patent No. 3,345,619, issued October 3, 1967, on an application filed October 21, 1964.

Footnote 4. U. S. Patent No. 3,351,917, issued November 7, 1967, on an application filed February 5, 1965.

Footnote 5. U. S. Patent No. 3,047,228, issued July 31, 1962.

Footnote 6. U. S. Patent No. 3,366,929, issued January 30, 1968, on an application filed December 30, 1964.

Footnote 7. This requirement is not involved in the case at bar, since the sole basis for the second paragraph rejection before us was that appellant was claiming something other than what he regarded as his invention. The rejection was not based on any lack of "definiteness" in the claims.

Footnote 8. See, e.g., Reviser's Note, 35 U.S.C.A. 112; H.R. Rep. No. 1923, 82nd Cong., 2d Sess. 19 (1952).

- End of Case -